Guidelines:

General Guidelines:

* Mechanical Board Dimension:
* Board Thickness: <= .5mm
* Impedance controlled routing
  + 50 Ohm Single Ended
  + 100 Ohm Differential
* Trace length matched routing for high-speed signals (These signals are listed under 'FGPA->Banks')
* 01005 Capacitors/Resistors can be placed on the bottom side of the board
* **PFETs and NFETs (Q?)** can be placed on the bottom side of the board
* T1 Can be on the bottom of board
* The pads for J2 can be moved to simplify routing
* Component S1 is locked

**Sheet Specific Guidelines:**

1. **Top:**
   1. Nothing
2. **Block Diagram**
   1. Nothing
3. **FPGA**
   1. Nothing
4. **FPGA Config**
   1. Nothing
5. **FPGA Banks**
   1. Place all capacitors to their respective banks/pins
   2. C61 should be placed close to Banks 0 and 1
   3. C60 should be placed close to Banks 2 and 3
6. **FPGA SERDES**
   1. Nothing
7. **FPGA Power**
   1. All bypass capacitors should be placed close to their respective pins
   2. The following signals are high speed differential and should be routed as 100 Ohms differential and the signals should be matched to within 10mils.
      1. TX\_P/TX\_N
      2. C\_TX\_P/C\_TX\_N
      3. TX\_CLK\_P/TX\_CLK\_N
      4. C\_TX\_CLK\_P/C\_TX\_CLK\_N
      5. RX\_P/RX\_N
      6. C\_RX\_P/C\_RX\_N
      7. RX\_CLK\_P/RX\_CLK\_N
      8. C\_RX\_CLK\_P/RX\_CLK\_N
   3. Please follow best practices when routing these high speed signals:
      1. Route over a solid plane
      2. where possible, the distance between differential traces (S) should be 2 X the distance between a differential trace (D):
         1. As an example if a differential trace has a space between the +/- of 4 mils. The distance between a separate differential trace should be 8 mils away from the first differential trace.
8. **Host Interface**
   1. Out of band resistors: R3, R4, R5, R6, R8, R10, R15, R31 should be placed on the tracks in a fly by fashion. The traces should pass underneath a pad and not in a ‘T’ configuration
   2. TVSs should be placed in a fly by fashion. The traces should pass underneath a pad and not in a ‘T’ configuration
9. **EPM**
   1. U4 (28V Boost Converter):
      1. Place C9 as close as possible to boost converter
      2. Place R13, R14 and C10 as close as possible to the IC
   2. All nets that carry power to the EPM should be as wide as possible, Nets include:
      1. V28P0
      2. EPMA
      3. EPMB
      4. EPMC
      5. EPMD
      6. GND
10. **Power**
    1. Place all bypass capacitors as close as possible to their respective regulators